

AMENDMENTS TO THE CLAIMS

Claims pending

- At time of the Action: Claims 1-67.
- After this Response: Claims 1-67.

Amended claims: 1, 3, 4-10, 14-21, 25-26, 29-31, 35-36, 38-39, 42-47, 50-53, 56, and 59-62.

Listing of Claims

1. (Currently amended) An apparatus that ~~uses~~ receives pseudo-differential voltage signaling including a common reference voltage and a plurality of signal voltages, comprising:

a reference receiver that receives ~~an undistributed~~ the common reference voltage of the pseudo-differential voltage signaling and in response produces a buffered voltage that is derived at least in part from the ~~undistributed~~ common reference voltage;

signal receivers associated respectively with ~~a plurality of~~ the one or more signal voltages;

wherein an individual signal receiver receives both its associated signal voltage and the buffered voltage~~[[,]]; and~~[[;]]

wherein said individual signal receiver evaluates its associated signal voltage and the buffered voltage to produce an output voltage.

2. (Original) An apparatus as recited in claim 1, wherein said individual signal receiver evaluates by comparing the associated signal voltage and the buffered voltage to produce an output voltage.

1
2 3. (Currently amended) An apparatus as recited in claim 1, wherein the
3 buffered voltage is the difference between the ~~undistributed~~-common reference
4 voltage and a distributed reference voltage.
5

6 4. (Currently amended) An apparatus as recited in claim 1, wherein the
7 buffered voltage is proportional to the ~~undistributed~~-common reference voltage.
8

9 5. (Currently amended) An apparatus as recited in claim 1, wherein the
10 buffered voltage represents the noise of the signal voltages relative to the
11 ~~undistributed~~-common reference voltage.
12

13 6. (Currently amended) An apparatus as recited in claim 1, wherein the
14 reference receiver also receives a distributed reference voltage that is received by
15 the signal receivers, wherein the reference receiver is responsive to the distributed
16 reference voltage and the ~~undistributed~~-common reference voltage to produce the
17 buffered voltage.
18

19 7. (Currently amended) An apparatus as recited in claim 1, wherein the
20 reference receiver also receives a distributed reference voltage that is received by
21 the signal receivers, wherein the reference receiver compares the distributed
22 reference voltage and the ~~undistributed~~-common reference voltage to produce the
23 buffered voltage.
24
25

1 8. (Currently amended) An apparatus as recited in claim 1, wherein the
2 reference receiver also receives a distributed reference voltage that is received by
3 the signal receivers, wherein the reference receiver compares the distributed
4 reference voltage and the ~~undistributed-common~~ reference voltage to produce the
5 buffered voltage, the buffered voltage representing the difference between the
6 distributed reference voltage and the ~~undistributed-common~~ reference voltage.

7
8 9. (Original) An apparatus as recited in claim 1, further comprising:
9 a plurality of signal buffers that receive the signal voltages and in response
10 produce buffered signal voltages, wherein each buffered signal voltage is subject
11 to a signal capacitance;

12 the buffered voltage being subject to a reference capacitance that is
13 ~~significantly~~ greater than the signal capacitance;

14 each of the signal buffers having a first electrical current capacity;

15 the reference receiver having a second electrical current capacity that is
16 greater than the first electrical current capacity by a ratio equal to the ratio of the
17 reference capacitance to the signal capacitance.

18
19 10. (Original) An apparatus as recited in claim 1, further comprising:

20 a plurality of signal buffers that receive the signal voltages and in response
21 produce buffered signal voltages, wherein each buffered signal voltage is subject
22 to a signal capacitance;

23 the buffered voltage being subject to a reference capacitance that is
24 ~~significantly~~ greater than the signal capacitance;

25 each of the signal buffers having a first electrical current capacity;

1 the reference receiver having a second electrical current capacity that is
2 greater than the first electrical current capacity by a ratio equal to the ratio of the
3 reference capacitance to the signal capacitance; and

4 wherein the reference receiver and the signal buffers are source-followers.

5
6 11. (Original) An apparatus as recited in claim 1, further comprising:
7 a plurality of signal buffers that receive the signal voltages and in response
8 produce buffered signal voltages.

9
10 12. (Original) An apparatus as recited in claim 1, further comprising:
11 a plurality of signal buffers that receive the signal voltages and in response
12 produce buffered signal voltages;

13 wherein the reference receiver and the signal buffers are source-followers.

14
15 13. (Original) An apparatus as recited in claim 1, wherein the reference
16 receiver has a unity gain.

17
18 14. (Currently amended) An apparatus as recited in claim 1, wherein:
19 the associated signal voltage of the individual signal receiver has associated
20 input capacitance and inductance that result in a resonant input frequency;

21 the reference receiver has a bandwidth that is ~~significantly~~ greater than the
22 resonant input frequency.

23
24 15. (Currently amended) An apparatus as recited in claim 1, wherein:
25

1 the associated signal voltage of the individual signal receiver has associated
2 input capacitance and inductance that result in a resonant input frequency; and
3 the reference receiver has a bandwidth of at least ten times the resonant
4 input frequency.

5
6 16. (Currently amended) An apparatus as recited in claim 1, wherein each
7 associated signal voltage represents one of two values and the signal receivers
8 compare the buffered voltage and the signal voltages to determine which of the
9 two values is represented by each associated signal voltage.

10
11 17. (Currently amended) An apparatus as recited in claim 1, the common
12 reference voltage and the buffered voltage being subject to similar impedances.

13
14 18. (Currently amended) An apparatus as recited in claim 1, the common
15 reference voltage[s] and associated signal voltage being subject to similar
16 impedances, wherein coupled signal noise is introduced approximately equally in
17 the buffered voltage and the plurality of pseudo-differential signal voltages, said
18 ~~approximately equal~~ coupled signal noise being canceled in the evaluation
19 performed by the signal receiver.

20
21 19. (Currently amended) An integrated circuit comprising:
22 a reference input that receives a common reference voltage;
23 a plurality of signal inputs configured to receive pseudo-differential signal
24 voltages that represent values in terms of relationships between the pseudo-
25 differential signal voltages and the common reference voltage;

1 a reference buffer that receives the common reference voltage and in
2 response produces a buffered reference voltage;

3 signal comparators associated respectively with the ~~plurality of~~ pseudo-
4 differential signal voltages, each signal comparator comparing the buffered
5 reference voltage and one of the pseudo-differential signal voltages to determine
6 the value represented by said one of the pseudo-differential signal voltages;

7 wherein the reference and signal inputs have similar impedances, coupled
8 signal noise being introduced approximately equally in the buffered reference
9 voltage and the ~~plurality of~~ pseudo-differential signal voltages, said ~~approximately~~
10 ~~equal~~ coupled signal noise being canceled in the comparison performed by the
11 signal comparators.

12
13 20. (Currently amended) An integrated circuit as recited in claim 19,
14 further comprising:

15 a plurality of signal buffers that receive the pseudo-differential signal
16 voltages and in response produce buffered signal voltages, wherein each buffered
17 signal voltage is subject to a signal capacitance;

18 the buffered reference voltage being subject to a reference capacitance that
19 is ~~significantly~~ greater than the signal capacitance;

20 each of the signal buffers having a first electrical current capacity;

21 the reference buffer having a second electrical current capacity that is
22 greater than the first electrical current capacity by a ratio equal to the ratio of the
23 reference capacitance to the signal capacitance.

24

25

1 21. (Currently amended) An integrated circuit as recited in claim 19,
2 further comprising:

3 a plurality of signal buffers that receive the pseudo-differential signal
4 voltages and in response produce buffered signal voltages, wherein each buffered
5 signal voltage is subject to a signal capacitance;

6 the buffered reference voltage being subject to a reference capacitance that
7 is ~~significantly~~ greater than the signal capacitance;

8 each of the signal buffers having a first electrical current capacity;

9 the reference buffer having a second electrical current capacity that is
10 greater than the first electrical current capacity by a ratio equal to the ratio of the
11 reference capacitance to the signal capacitance; and

12 wherein the reference buffer and the signal buffers are source-followers.
13

14 22. (Original) An integrated circuit as recited in claim 19, further
15 comprising:

16 a plurality of signal buffers that receive the pseudo-differential signal
17 voltages and in response produce buffered signal voltages for comparison by the
18 signal comparators.
19

20 23. (Original) An integrated circuit as recited in claim 19, further
21 comprising:

22 a plurality of signal buffers that receive the pseudo-differential signal
23 voltages and in response produce buffered signal voltages;

24 wherein the reference buffer and the signal buffers are source-followers.
25

1 24. (Original) An integrated circuit as recited in claim 19, wherein the
2 reference buffer has a unity gain.

3
4 25. (Currently amended) An integrated circuit as recited in claim 19,
5 wherein:

6 the signal inputs have associated input capacitances and inductances that
7 result in a resonant input frequency;

8 the reference buffer has a bandwidth that is ~~significantly~~ greater than the
9 resonant input frequency.

10
11 26. (Currently amended) An integrated circuit as recited in claim 19,
12 wherein:

13 the plurality of signal inputs ha[[s]]ve associated input capacitances and
14 inductances that result in [[a]] resonant input frequenc[[y]]ies; and

15 the reference buffer has a bandwidth of at least ten times the resonant input
16 frequency.

17
18 27. (Original) An integrated circuit as recited in claim 19, wherein each
19 signal voltage represents one of two values and the signal comparators compare
20 the buffered reference voltage and the signal voltages to determine which of the
21 two values is represented by each signal voltage.

22
23 28. (Original) An integrated circuit as recited in claim 19, the reference and
24 signal inputs having matching impedances.

1 29. (Currently amended) A system comprising:

2 a first integrated circuit that transmits a common reference voltage and a
3 plurality of pseudo-differential signal voltages, wherein the plurality of pseudo-
4 differential signal voltages represent values in terms of relationships between the
5 plurality of pseudo-differential signal voltages and the common reference voltage;

6 a second integrated circuit that receives the common reference voltage and
7 the plurality of pseudo-differential signal voltages;

8 the second integrated circuit having a reference buffer that receives the
9 common reference voltage and in response produces a buffered reference voltage;

10 the second integrated circuit having signal comparators associated
11 respectively with the plurality of pseudo-differential signal voltages, each signal
12 comparator comparing the buffered reference voltage and a respective one of the
13 plurality of pseudo-differential signal voltages to determine the value represented
14 by said one of the plurality of pseudo-differential signal voltages;

15 wherein the second integrated circuit is configured to introduce
16 approximately equal coupled signal noise in the buffered reference voltage and the
17 plurality of pseudo-differential signal voltages, said approximately equal coupled
18 signal noise being canceled in the comparisons performed by the signal
19 comparators.

20
21 30. (Currently amended) A system as recited in claim 29, the second
22 integrated circuit further comprising:

23 a plurality of signal buffers that receive the pseudo-differential signal
24 voltages and in response produce buffered signal voltages, wherein each buffered
25 signal voltage is subject in the second integrated circuit to a signal capacitance;

1 the buffered reference voltage being subject in the second integrated circuit
2 to a reference capacitance that is ~~significantly~~ greater than the signal capacitance;
3 each of the signal buffers having a first electrical current capacity;
4 the reference buffer having a second electrical current capacity that is
5 greater than the first electrical current capacity by a ratio equal to the ratio of the
6 reference capacitance to the signal capacitance.

7
8 31. (Currently amended) A system as recited in claim 29, the second
9 integrated circuit further comprising:

10 a plurality of signal buffers that receive the pseudo-differential signal
11 voltages and in response produce buffered signal voltages, wherein each buffered
12 signal voltage is subject in the second integrated circuit to a signal capacitance;

13 the buffered reference voltage being subject in the second integrated circuit
14 to a reference capacitance that is ~~significantly~~ greater than the signal capacitance;

15 each of the signal buffers having a first electrical current capacity;

16 the reference buffer having a second electrical current capacity that is
17 greater than the first electrical current capacity by a ratio equal to the ratio of the
18 reference capacitance to the signal capacitance; and

19 wherein the reference buffer and the signal buffers are source-followers.

20
21 32. (Original) A system as recited in claim 29, the second integrated circuit
22 further comprising:

23 a plurality of signal buffers that receive the pseudo-differential signal
24 voltages and in response produce buffered signal voltages.

25

1 33. (Original) A system as recited in claim 29, the second integrated circuit
2 further comprising:

3 a plurality of signal buffers that receive the pseudo-differential signal
4 voltages and in response produce buffered signal voltages;
5 wherein the reference buffer and the signal buffers are source-followers.
6

7 34. (Original) A system as recited in claim 29, wherein the reference buffer
8 is a unity gain amplifier.
9

10 35. (Currently amended) A system as recited in claim 29, wherein:
11 the second integrated circuit has signal inputs that receive the plurality of
12 pseudo-differential signal voltages, the signal inputs having associated input
13 capacitance and inductance that result in a resonant input frequency;
14 the reference buffer has a bandwidth that is ~~significantly~~ greater than the
15 resonant input frequency.
16

17 36. (Currently amended) A system as recited in claim 29, wherein:
18 the second integrated circuit has signal inputs that receive the plurality of
19 pseudo-differential signal voltages, the signal inputs having associated input
20 capacitance and inductance that result in a resonant input frequency; and
21 the reference buffer has a bandwidth of at least ten times the resonant input
22 frequency.
23

24 37. (Original) A system as recited in claim 29, wherein each pseudo-
25 differential signal voltage represents one of two values and the comparators

1 compare the buffered reference voltage and the pseudo-differential signal voltages
2 to determine which of the two values is represented by each pseudo-differential
3 signal voltage.

4
5 38. (Currently amended) A system as recited in claim 29, wherein the
6 second integrated circuit has signal inputs that receive the pseudo-differential
7 signal voltages and a reference input that receives the common reference voltage,
8 the reference input and signal inputs having similar impedances.

9
10 39. (Currently Amended) A method comprising:
11 ~~receiving a reference voltage;~~
12 receiving pseudo-differential signaling that includes a common reference
13 voltage and a plurality of signal voltages;
14 producing a buffered voltage based at least in part on the common reference
15 voltage;
16 evaluating the buffered voltage and one of the signal voltages to determine
17 a value represented by said one of the signal voltages.

18
19 40. (Original) A method as recited in claim 39, wherein the evaluating
20 comprises comparing said one of the signal voltages and the buffered voltage to
21 produce an output voltage.

22
23 41. (Original) A method as recited in claim 39, wherein the buffered
24 voltage is the difference between an undistributed reference voltage and a
25 distributed reference voltage.

1
2 42. (Currently amended) A method as recited in claim 39, wherein the
3 buffered voltage is proportional to the common reference voltage.
4

5 43. (Original) A method as recited in claim 39, wherein the buffered
6 voltage represents the noise of the signal voltages.
7

8 44. (Currently amended) A method as recited in claim 39, said producing
9 comprising comparing a distributed reference voltage that is received by [[the]]
10 signal receivers and an undistributed reference voltage that is not received by the
11 signal receivers.
12

13 45. (Currently amended) A method as recited in claim 39, said producing
14 comprising comparing a distributed reference voltage that is received by [[the]]
15 signal receivers and an undistributed reference voltage that is not received by the
16 signal receivers, the buffered voltage representing the difference between the
17 undistributed reference voltage and the distributed reference voltage.
18

19 46. (Currently amended) A method as recited in claim 39, further
20 comprising:

21 buffering the signal voltages with signal buffers to produce buffered signal
22 voltages, wherein each buffered signal voltage is subject to a signal capacitance;

23 said producing the buffered voltage being performed with a reference
24 buffer, the buffered voltage being subject to a reference capacitance that is
25 ~~significantly~~ greater than the signal capacitance;

1 each of the signal buffers having a first electrical current capacity;
2 the reference buffer having a second electrical current capacity that is
3 greater than the first electrical current capacity by a ratio equal to the ratio of the
4 reference capacitance to the signal capacitance.
5

6 47. (Currently amended) A method as recited in claim 39, further
7 comprising:

8 buffering the signal voltages with source-follower signal buffers to produce
9 buffered signal voltages, wherein each buffered signal voltage is subject to a signal
10 capacitance;

11 said producing the buffered voltage being performed with a source-follower
12 reference buffer, the buffered voltage being subject to a reference capacitance that
13 is significantly greater than the signal capacitance;

14 each of the signal buffers having a first electrical current capacity;
15 the reference buffer having a second electrical current capacity that is
16 greater than the first electrical current capacity by a ratio equal to the ratio of the
17 reference capacitance to the signal capacitance.
18

19 48. (Original) A method as recited in claim 39, further comprising:
20 buffering the signal voltages to produce buffered signal voltages.
21

22 49. (Original) A method as recited in claim 39, further comprising:
23 buffering the signal voltages with source-followers to produce buffered
24 signal voltages.
25

1 50. (Currently amended) A method as recited in claim 39, wherein:
2 the signal voltages are received by signal inputs having associated input
3 capacitances and inductances that define a resonant frequency;
4 producing the buffered voltage with a unity gain buffer having a bandwidth
5 that is ~~significantly~~ greater than the resonant frequency.

6
7 51. (Currently amended) A method as recited in claim 39, wherein:
8 the signal voltages are received by signal inputs having associated input
9 capacitances and inductances that define a resonant input frequency; and
10 producing the buffered voltage is performed with a unity gain buffer having
11 a bandwidth of at least ten times the resonant input frequency.

12
13 52. (Currently amended) A method as recited in claim 39, wherein:
14 the common reference voltage is received by a reference input;
15 the signal voltages are received by signal inputs; and
16 the reference and signal inputs have similar impedances.

17
18 53. (Currently amended) A method as recited in claim 39, further
19 comprising introducing coupled signal noise approximately equally in the buffered
20 reference voltage and the plurality of signal voltages, said ~~approximately equal~~
21 coupled signal noise being canceled in the comparing.

22
23 54. (Original) An apparatus that uses pseudo-differential voltage signaling,
24 comprising:
25 signal receivers associated respectively with a plurality of signal voltages;

1 a reference receiver that receives both an undistributed reference voltage
2 and a distributed reference voltage, wherein the distributed reference voltage is
3 distributed to the signal receivers and the undistributed reference voltage is not
4 distributed to the signal receivers;

5 wherein the reference receiver evaluates the undistributed reference voltage
6 and the distributed reference voltage to produce a buffered voltage that represents
7 the difference between the undistributed reference voltage and the distributed
8 reference voltage;

9 wherein an individual signal receiver receives both its associated signal
10 voltage and the buffered voltage; and

11 wherein said individual signal receiver adjusts its associated signal voltage
12 by the buffered voltage to produce an output voltage.

13
14 55. (Original) An apparatus as recited in claim 54, wherein said signal
15 receivers are two-stage receivers.

16
17 56. (Currently amended) An apparatus as recited in claim 54, wherein said
18 signal receivers are two-stage receivers, wherein ~~[[the]]~~ a second stage of the
19 signal receivers adjust~~[[ing]]~~s ~~[[the]]~~ signal voltage~~[[s]]~~.

20
21 57. (Original) An apparatus as recited in claim 54, wherein the buffered
22 voltage represents the noise of the signal voltages relative to the undistributed
23 reference voltage.

1 58. (Original) An apparatus as recited in claim 54, wherein the buffered
2 voltage is a differential voltage.

3
4 59. (Currently amended) An integrated circuit that uses pseudo-differential
5 voltage signaling, comprising:

6 two-stage receivers associated respectively with a plurality of signal
7 voltages;

8 a reference receiver that receives both an undistributed reference voltage
9 and a distributed reference voltage, wherein the distributed reference voltage is
10 distributed to the ~~signal~~two-stage receivers and the undistributed reference voltage
11 is not distributed to the signal receivers;

12 wherein the reference receiver compares the undistributed reference voltage
13 and the distributed reference voltage to produce a buffered voltage that represents
14 the difference between the undistributed reference voltage and the distributed
15 reference voltage;

16 wherein the first stage of an individual signal receiver compares its
17 associated signal voltage to the distributed reference voltage to produce a voltage
18 differential signal; and

19 wherein the second stage of said individual two-stage receiver adjusts the
20 voltage differential signal by the buffered voltage to produce an output voltage.

21
22 60. (Currently amended) An ~~apparatus~~integrated circuit as recited in claim
23 59, the two-stage receivers ~~have~~ha[[s]]ve an input impedance similar to that of the
24 reference receiver.

1 61. (Currently amended) An ~~apparatus~~integrated circuit as recited in claim
2 59, wherein the buffered voltage represents the noise of the signal voltages relative
3 to the undistributed reference voltage.

4
5 62. (Currently amended) An ~~apparatus~~integrated circuit as recited in claim
6 59, wherein the buffered voltage is a differential voltage.

7
8 63. (Original) A system comprising:
9 a first integrated circuit that transmits a common reference voltage and a
10 plurality of pseudo-differential signal voltages, wherein the pseudo-differential
11 signal voltages represent values in terms of relationships between the pseudo-
12 differential signal voltages and the common reference voltage;

13 a second integrated circuit that receives the common reference voltage and
14 the plurality of pseudo-differential signal voltages;

15 the second integrated circuit having a reference receiver that receives the
16 common reference voltage and in response produces a buffered voltage;

17 the second integrated circuit having two-stage signal receivers associated
18 respectively with the plurality of pseudo-differential signal voltages, each two-
19 stage signal receiver adjusting one of the pseudo-differential signal voltages by the
20 buffered voltage to produce an output voltage.

21
22 64. (Original) A system as recited in claim 63, wherein each two-stage
23 signal receiver has an input impedance similar to that of the reference receiver.

24
25 65. (Original) A system as recited in claim 63, wherein:

1 the reference receiver compares a distributed common reference voltage to
2 an undistributed common reference voltage to produce the buffered voltage;

3 the first stage of an individual two-stage signal receiver compares its
4 associated pseudo-differential signal voltage to a distributed reference voltage to
5 produce a voltage differential signal; and

6 the second stage of said individual two-stage signal receiver adjusts the
7 voltage differential signal by the buffered voltage to produce an output voltage.

8
9 66. (Original) A system as recited in claim 63, wherein the buffered voltage
10 represents the noise of the signal voltages.

11
12 67. (Original) A system as recited in claim 63, wherein the buffered voltage
13 is a differential voltage.